Objective:

The objective of this lab is to design and implant the hand-ball timer on DE-01 FPGA board. Different Seven segment displays are used to show the timer. Hex0 and Hex1 is used to show the seconds while Hex2 and Hex3 are used to show minutes. Hex4 and Hex 5 are used to show the first and second half.

Procedure

A top-level entity consists of control logic which is providing the necessary signals to counter module. Counter module is counting the minutes and second and passing them to seven segment which is controller by bcd to seven segment entity. The schematic and simulation results of each module is shown.

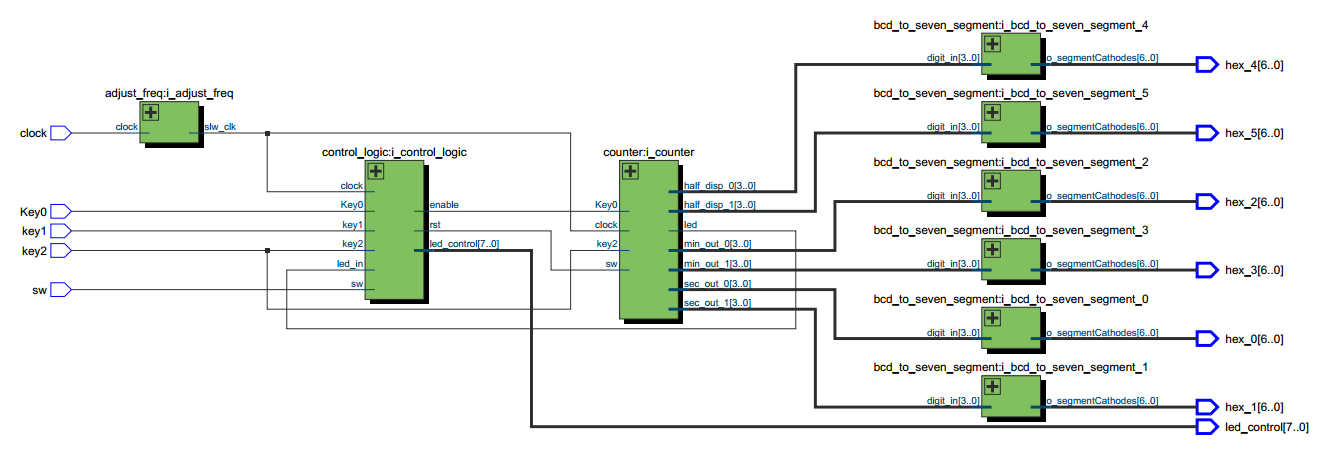


Figure : RTL Schematic

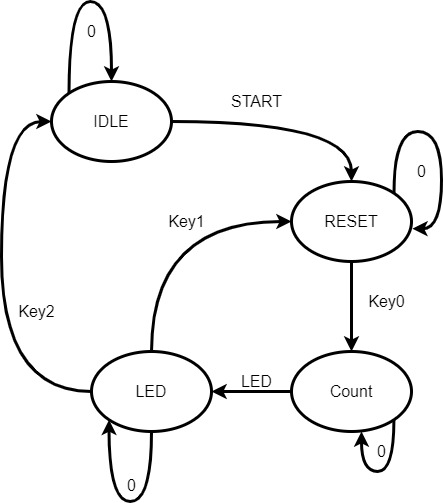


Figure 2: FSM of counter

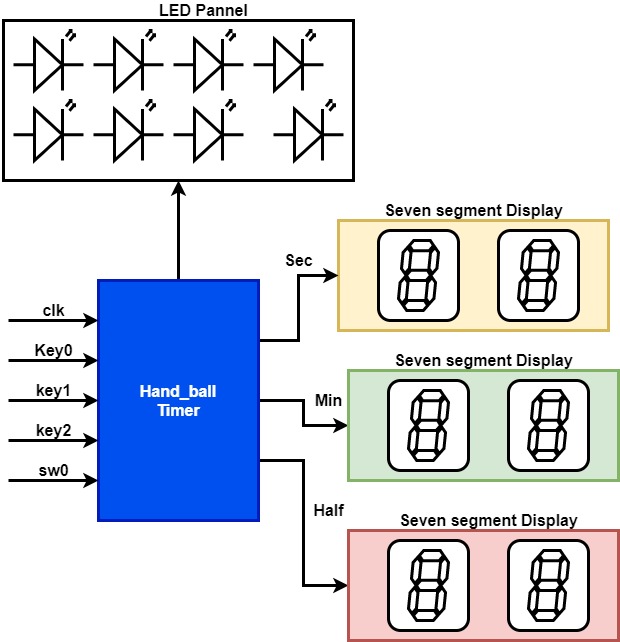


Figure 3: System level diagram

Results:

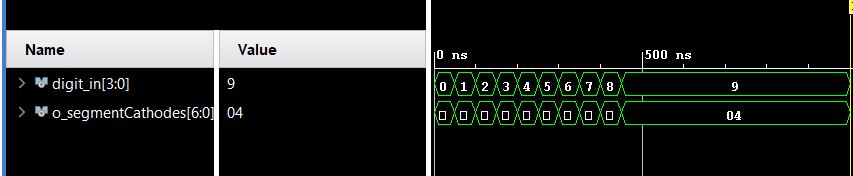


Figure 4: BCD seven

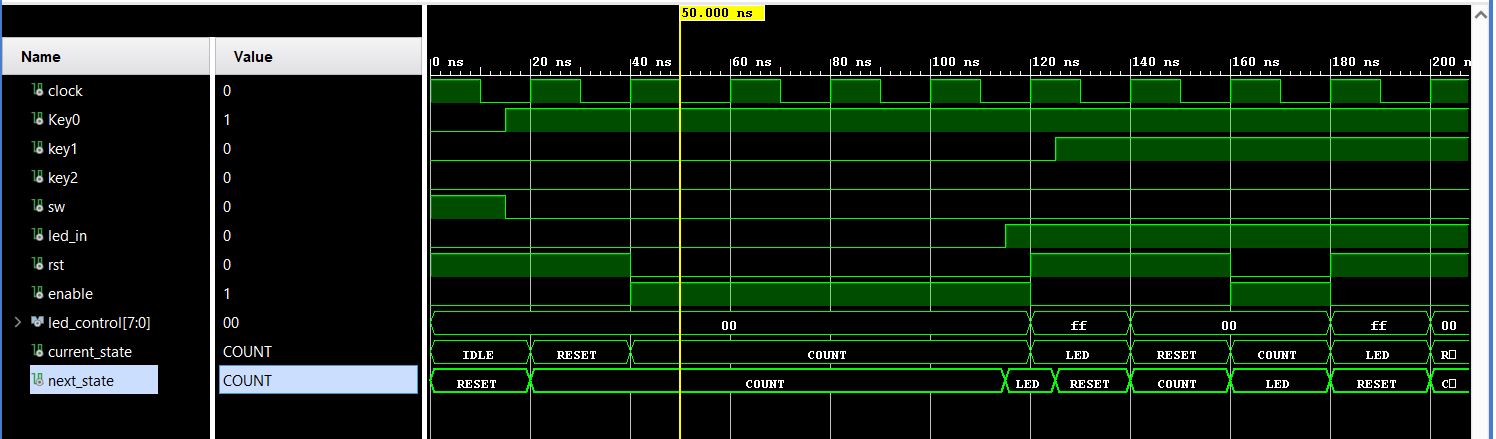


Figure 5: Control logic

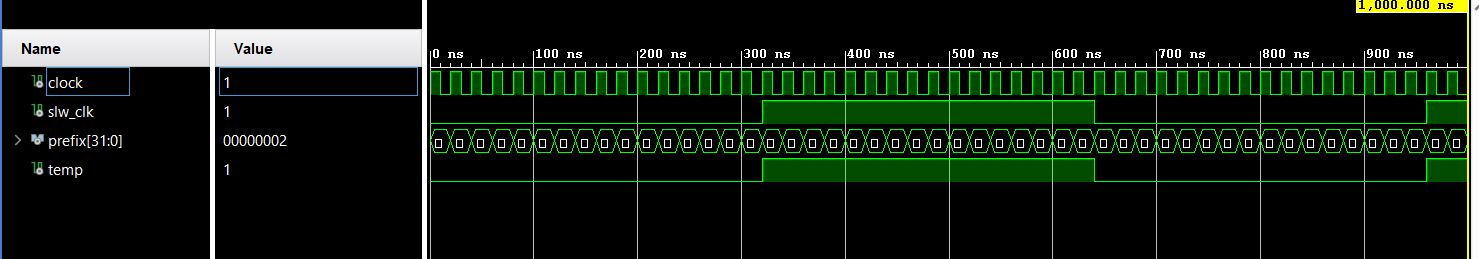


Figure 6: slow clock

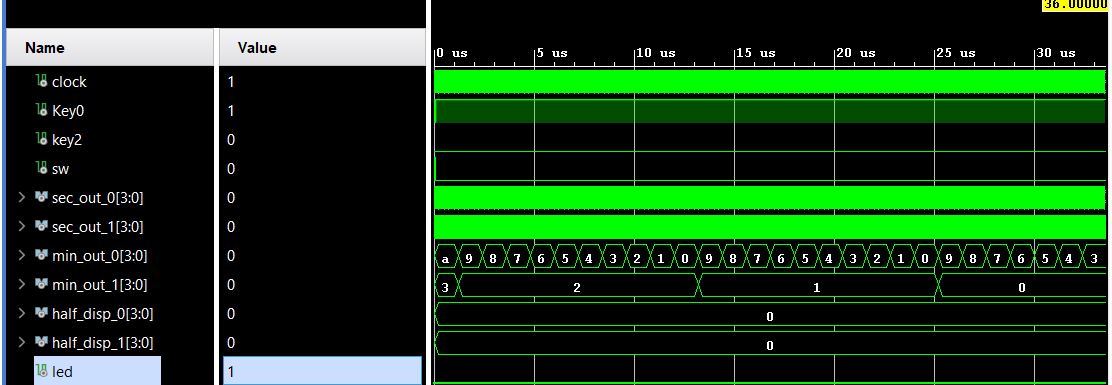


Figure 7: counter

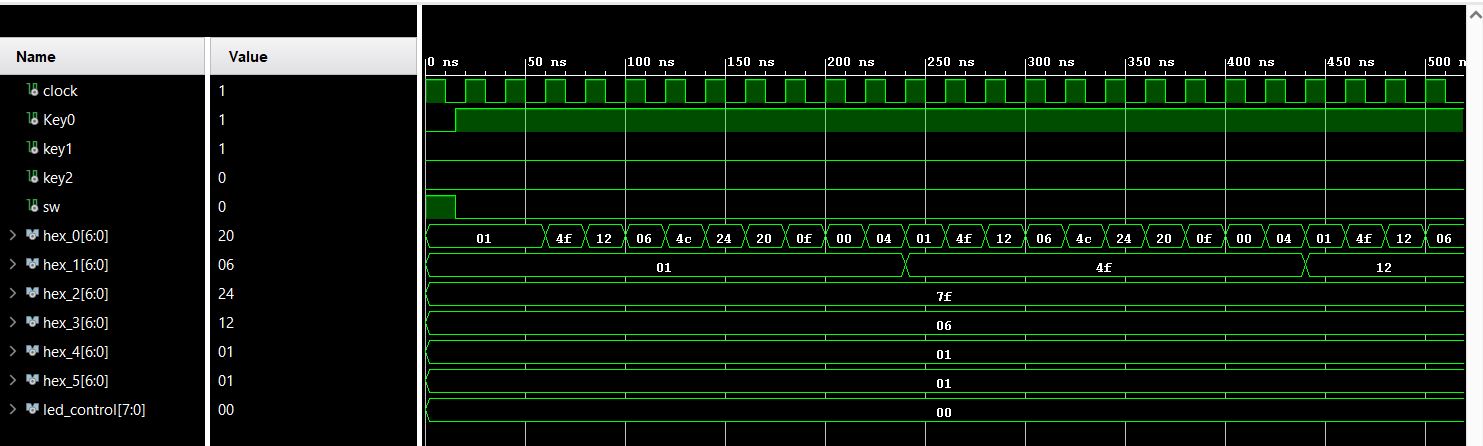


Figure : Top level